Dead Time Calculations

Overview

The total dead time is governed by the turn OFF delay of Q1B. Q1B has the longest turn OFF delay compared to Q1A. The total time delay to fully turn OFF Q1B is from the MCU execution (code to outpin realization) to the turn OFF of Q2 and finally the turn OFF of Q1B. The following analysis considers all the possible delay incurred.

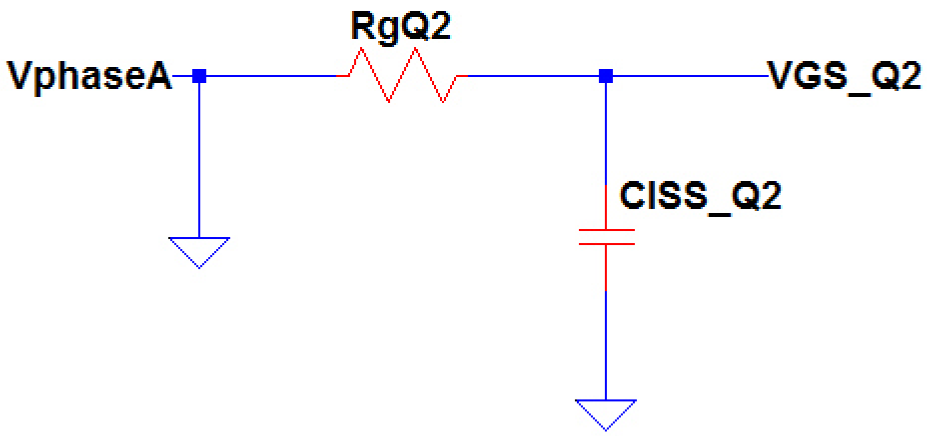
I made an excel tool to calculate the dead time specific for this application. You can enter values on it and the dead time is automatically computed.This is very useful if you want to change parts wherein there are changes in the parameters involved.

Total Turn OFF Delay of Q1B (same with other upper MOSFETs)

Q2 Turn OFF delay

When Q2 is running ON, its gate to source is supplied by the phaseA voltage which is coming from the MCU. Once the MCU command turn OFF by pulling the phaseA to low, the input capacitance of Q2 will discharge through the gate resistance of Q2.

Circuit model for analysis



Q2 will turn OFF only when the level of VGS_Q2 is below the gate to source threshold voltage.The level of VGS_Q2 will follow the exponential decay equation below.

$$\mathrm{VGS\_Q2} = \mathrm{VGS\_Q2\_initial}\cdot e^{\frac{-\,\mathrm{tdecay\_Q2gate}}{\mathrm{RgQ2}\cdot \mathrm{CISS\_Q2}}}$$

solving for tdecay_Q2gate

$$\mathrm{VGS\_Q2} = \mathrm{VGS\_Q2\_initial}\cdot e^{\frac{-\,\mathrm{tdecay\_Q2gate}}{\mathrm{RgQ2}\cdot\mathrm{CISS\_Q2}}}\ \ \mathrm{solve}, \mathrm{tdecay\_Q2gate}\ \rightarrow -\mathrm{CISS\_Q2}\cdot\mathrm{RgQ2}\cdot\ln\left(\frac{\mathrm{VGS\_Q2}}{\mathrm{VGS\_Q2\_initial}}\right)$$

$$\mathrm{tdecay\_Q2gate} = -\mathrm{CISS\_Q2}\cdot\mathrm{RgQ2}\cdot\ln\left(\frac{\mathrm{VGS\_Q2}}{\mathrm{VGS\_Q2\_initial}}\right)$$

where;

- tdecay_Q2gate is the time needed so that the input capacitance charge is no longer enough to hold Q2 in the ON state condition.
- VGS_Q2 is the instantaneous level of the gate to source voltage
- VGS_Q2_initial is the gate to surce voltage when Q2 is at ON state. Since the gate to souce resistance of a MOSFET is very high, the voltage dividing effect of RgQ2 is very negligible. Thus VGS_Q2_initial is equal to the level of VphaseA. So

$$\mathrm{VGS\_Q2\_initial} = \mathrm{VphaseA}$$

$$\mathrm{tdecay\_Q2gate} = -\mathrm{CISS\_Q2}\cdot\mathrm{RgQ2}\cdot\ln\left(\frac{\mathrm{VGS\_Q2}}{\mathrm{VGS\_Q2\_initial}}\right)$$

$$\mathrm{tdecay\_Q2gate} = -\mathrm{CISS\_Q2}\cdot\mathrm{RgQ2}\cdot\ln\left(\frac{\mathrm{VGS\_Q2}}{\mathrm{VphaseA}}\right)$$

To turn OFF Q2, the level of VGS_Q2 must be below the minimum threshold level. So,

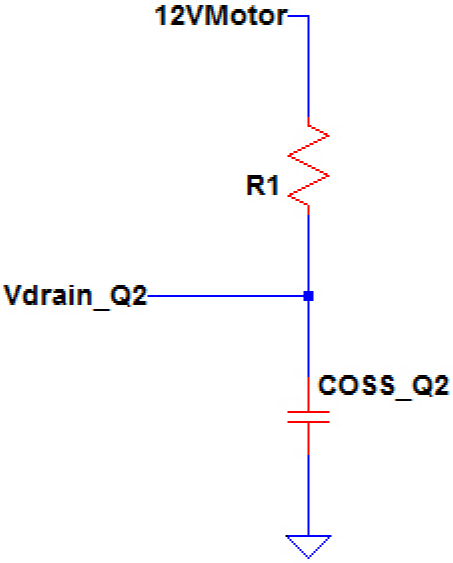
$$\mathrm{tdecay\_Q2gate} = -\mathrm{CISS\_Q2}\cdot\mathrm{RgQ2}\cdot\ln\left(\frac{\mathrm{VGS\_Q2}}{\mathrm{VphaseA}}\right)$$

$$\mathrm{tdecay\_Q2gate} = -\mathrm{CISS\_Q2}\cdot\mathrm{RgQ2}\cdot\ln\left(\frac{\mathrm{VGS\_Q2threshold\_min}}{\mathrm{VphaseA}}\right)$$

Q1B Turn OFF Delay

Q1B will turn OFF only when the difference of 12VMotor and the drain voltage of Q2 is below the source to gate threshold voltage. I am using here the words "source to gate voltage" since this is PMOS.

When the gate to source voltage of Q2 is below the threshold level, the COSS of Q2 will start to charge through R1. The circuit model for analysis is given below



The Vdrain_Q2 will follow the exponential rise equation as below

$$\text{Vdrain\_Q2} = \text{Vfullcharge} \cdot \left(1 - e^{\frac{-\text{trise\_Q2drain}}{\text{R1} \cdot \text{COSS\_Q2}}}\right)$$

solve for trise_Q2drain

$$\text{Vdrain\_Q2} = \text{Vfullcharge}\cdot\left(1 - e^{\frac{-\,\text{trise\_Q2drain}}{\text{R1}\cdot\text{COSS\_Q2}}}\right)\ \text{solve}, \text{trise\_Q2drain}\ \rightarrow -\text{COSS\_Q2}\cdot\text{R1}\cdot\ln\left(1 - \frac{\text{Vdrain\_Q2}}{\text{Vfullcharge}}\right)$$

$$\text{trise\_Q2drain} = -\text{COSS\_Q2}\cdot\text{R1}\cdot\ln\left(1 - \frac{\text{Vdrain\_Q2}}{\text{Vfullcharge}}\right)$$

where;

- trise_Q2drain is the time delay wherein Q1B source to gate voltage become below the threshold level
- COSS_Q2 is the output capacitance of Q2
- Vdrain_Q2 is the instantaneous drain voltage of Q2
- Vfullcharge is the full charge voltage of the COSS of Q2. At full charge level, the dividing effect of R1 is negligible so Vfullcharge is equal to the level of 12VMotor. So

$$\text{Vfullcharge} = \text{V12VMotor}$$

$$\text{trise\_Q2drain} = -\text{COSS\_Q2}\cdot\text{R1}\cdot\ln\left(1 - \frac{\text{Vdrain\_Q2}}{\text{Vfullcharge}}\right)$$

$$\text{trise\_Q2drain} = -\text{COSS\_Q2}\cdot\text{R1}\cdot\ln\left(1 - \frac{\text{Vdrain\_Q2}}{\text{V12VMotor}}\right)$$

The input capacitance of Q1B is also preventing the source to gate voltage to decay to zero that fast. So it must be condidered as well.

$$\text{tdecay\_Q1Bgate} = -\text{CISS\_Q1B}\cdot\text{RgQ1B}\cdot\ln\left(\frac{\text{VSG\_Q1B}}{\text{VSG\_Q2\_initial}}\right)$$

The initial level of the source to gate voltage (VSG_Q2_initial) is equal to the level of 12VMotor because Q2 is saturating during this time. So

$$\text{tdecay\_Q1Bgate} = -\text{CISS\_Q1B}\cdot\text{RgQ1B}\cdot\ln\left(\frac{\text{VSG\_Q1B}}{\text{V12VMotor}}\right)$$

Q1B will fully turn OFF when its source to gate voltage is already below the threshold level, so

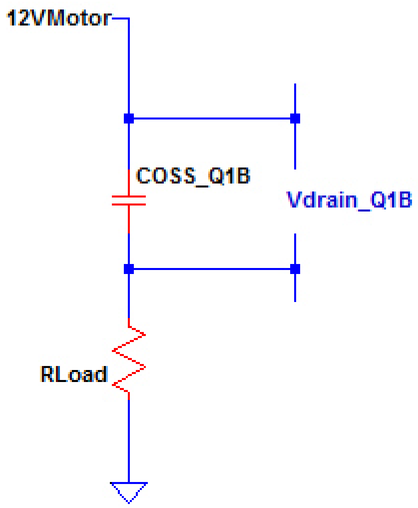
$$\mathrm{tdecay\_Q1Bgate} = -\mathrm{CISS\_Q1B} \cdot \mathrm{RgQ1B} \cdot \ln\left(\frac{\mathrm{VSG\_Q1B\_min}}{\mathrm{V12VMotor}}\right)$$

When Vdrain_Q2 is less then to the difference of V12VMotor and the minimum source to gate voltage of Q1B, the COSS of Q1B will start to charge. So we can re-write the above equation as below.

$$\mathrm{trise\_Q2drain} = -\mathrm{COSS\_Q2} \cdot \mathrm{R1} \cdot \ln\left(1 - \frac{\mathrm{Vdrain\_Q2}}{\mathrm{V12VMotor}}\right)$$

$$\mathrm{trise\_Q2drain} = -\mathrm{COSS\_Q2} \cdot \mathrm{R1} \cdot \ln\left(1 - \frac{\mathrm{V12VMotor} - \mathrm{VSG\_Q1B\_min}}{\mathrm{V12VMotor}}\right)$$

When the source to gate voltage of Q1B is below the required level for operation, Q1B COSS will start to charge until it reaches the full charge level which is ideally equal to the level of 12V Motor. since the dividing effect of the load is negligible.



The charging of the COSS of Q1B follows exponential rise given by below equation.

$$\mathrm{Vdrain\_Q1B} = \mathrm{V12VMotor}\cdot\left(1 - e^{\frac{-\,\mathrm{trise\_Q1Bdrain}}{\mathrm{RLoad}\cdot\mathrm{COSS\_Q1B}}}\right)$$

solve for trise_Q1Bdrain

$$\mathrm{Vdrain\_Q1B} = \mathrm{V12VMotor}\cdot\left(1 - e^{\frac{-\,\mathrm{trise\_Q1Bdrain}}{\mathrm{RLoad}\cdot\mathrm{COSS\_Q1B}}}\right)\ \mathrm{solve}, \mathrm{trise\_Q1Bdrain}\ \rightarrow -\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}\cdot\ln\left(1 - \frac{\mathrm{Vdrain\_Q1B}}{\mathrm{V12VMotor}}\right)$$

$$\mathrm{trise\_Q1Bdrain} = -\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}\cdot\ln\left(1 - \frac{\mathrm{Vdrain\_Q1B}}{\mathrm{V12VMotor}}\right)$$

We want to turn ON the lower MOSFET when the drain voltage of Q1B is already at the maximum in order to be sure no overlap. So, Vdrain_Q1B in the above equation should be equal to the level of V12VMotor. Re-writing the equation will give

$$\mathrm{trise\_Q1Bdrain} = -\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}\cdot\ln\left(1 - \frac{\mathrm{Vdrain\_Q1B}}{\mathrm{V12VMotor}}\right)$$

$$\mathrm{trise\_Q1Bdrain} = -\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}\cdot\ln\left(1 - \frac{\mathrm{V12VMotor}}{\mathrm{V12VMotor}}\right)$$

The above equation will result an error since the natural logarithm of 0 is undefined. In reality, 5 time constant is already a treated as a settling state of an exponential waveform. At 5 time constant, the level of Vdrain_Q1B is already at 99.32% of V12VMotor. So,

$$\mathrm{trise\_Q1Bdrain} = -\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}\cdot\ln\left(1 - \frac{\mathrm{V12VMotor}}{\mathrm{V12VMotor}}\right)$$

$$\mathrm{trise\_Q1Bdrain} = -\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}\cdot\ln\left(1 - \frac{0.9932\cdot\mathrm{V12VMotor}}{\mathrm{V12VMotor}}\right)$$

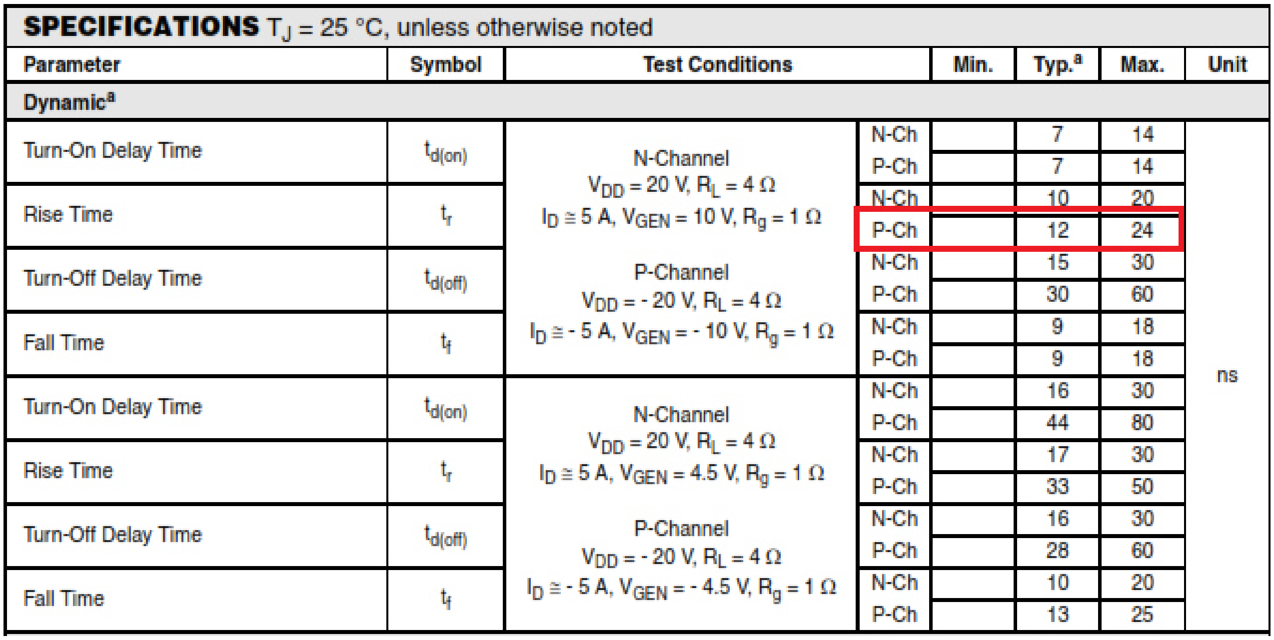
$$\mathrm{trise\_Q1Bdrain} = 4.990832666800076037\cdot\mathrm{COSS\_Q1B}\cdot\mathrm{RLoad}$$

This is based on the charging of the COSS

Above equaton is simply 5tau.

The datasheet also specified a rise time delay when the MOSFET is to be used as a high frequency switch as below. For worst case, we can add this as well. So

trise_Q1Bdynamic := 24ns



SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions		Min.	Typ.[a]	Max.	Unit
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 20 V, R_L = 4 Ω I_D ≅ 5 A, V_{GEN} = 10 V, R_g = 1 Ω P-Channel V_{DD} = - 20 V, R_L = 4 Ω I_D ≅ - 5 A, V_{GEN} = - 10 V, R_g = 1 Ω	N-Ch		7	14	ns
			P-Ch		7	14	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		12	24	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		15	30	
			P-Ch		30	60	
Fall Time	t_f		N-Ch		9	18	
			P-Ch		9	18	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 20 V, R_L = 4 Ω I_D ≅ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = - 20 V, R_L = 4 Ω I_D ≅ - 5 A, V_{GEN} = - 4.5 V, R_g = 1 Ω	N-Ch		16	30	
			P-Ch		44	80	
Rise Time	t_r		N-Ch		17	30	
			P-Ch		33	50	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		16	30	
			P-Ch		28	60	
Fall Time	t_f		N-Ch		10	20	
			P-Ch		13	25	

Solving for the total delay to turn OFF Q1B

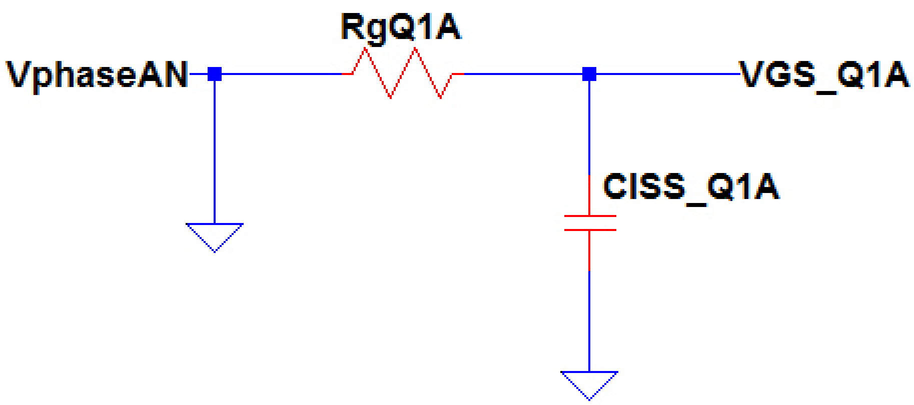
The total delay to fully turn OFF Q1B and its drain to source voltage is at the resting level is the sum of the computed individual delays above plus the microcontroller execution delay.

toff_Q1B_total **=** tdecay_Q2gate + trise_Q2drain + tdecay_Q1Bgate + trise_Q1Bdrain + MCUdelay

MCU delay is the time delay from the code to the realization in the output pin. I assumed MCU delay in this document. If you want to change MCU delay or any other parament, you can do the recomputation in the excel dead time calculator I made specific for this.

Total Turn OFF Delay of Q1A (same with other lower MOSFETs)

Q1A will turn OFF when its gate to source voltage is less than the required threshold. By the moment the micro pull down the phaseAN to low, the input capacitance of Q1A will discharge to the gate resistance of the device.



The working equation is following an exponential decay

$$\mathrm{VGS\_Q1A} = \mathrm{VGS\_Q1A\_initial} \cdot e^{\frac{-\mathrm{tdecay\_Q1Agate}}{\mathrm{RgQ1A} \cdot \mathrm{CISS\_Q1A}}}$$

solving for tdecay_Q1Agate

$$\text{VGS\_Q1A} = \text{VGS\_Q1A\_initial}\cdot e^{\frac{-\,\text{tdecay\_Q1Agate}}{\text{RgQ1A}\cdot\text{CISS\_Q1A}}}$$

$$\text{VGS\_Q1A} = \text{VGS\_Q1A\_initial}\cdot e^{\frac{-\,\text{tdecay\_Q1Agate}}{\text{RgQ1A}\cdot\text{CISS\_Q1A}}} \text{ solve, tdecay\_Q1Agate } \rightarrow -\text{CISS\_Q1A}\cdot\text{RgQ1A}\cdot\ln\left(\frac{\text{VGS\_Q1A}}{\text{VGS\_Q1A\_initial}}\right)$$

$$\text{tdecay\_Q1Agate} = -\text{CISS\_Q1A}\cdot\text{RgQ1A}\cdot\ln\left(\frac{\text{VGS\_Q1A}}{\text{VGS\_Q1A\_initial}}\right)$$

As mentioned, to fully turn OFF Q1A its applied gate to source voltage must become lower than the threshold level. So,

$$\text{tdecay\_Q1Agate} = -\text{CISS\_Q1A}\cdot\text{RgQ1A}\cdot\ln\left(\frac{\text{VGS\_Q1A}}{\text{VGS\_Q1A\_initial}}\right)$$

$$\text{tdecay\_Q1Agate} = -\text{CISS\_Q1A}\cdot\text{RgQ1A}\cdot\ln\left(\frac{\text{VGS\_Q1Athreshold\_min}}{\text{VGS\_Q1A\_initial}}\right)$$

When the CISS_Q1A (when the FET is at ON state) is at full level, VGS_Q1A_initial is just the level of phaseAN since the dividing effect of RgQ1A is very negligible. Thus,

$$\text{tdecay\_Q1Agate} = -\text{CISS\_Q1A}\cdot\text{RgQ1A}\cdot\ln\left(\frac{\text{VGS\_Q1Athreshold\_min}}{\text{VphaseAN}}\right)$$

When the applied VGS of Q1A is no longer enough to sustain turn ON operation, the device will turn OFF. By the moment Q1A turns OFF, its drain to source voltage will not charge higher than zero since during this time there is no path to the 12VMotor. Instead, the drain of Q1A will clamp to the negative body diode level because the motor load is inductive (there is something like reverse voltage from the motor inductance, this is based on simulation model). Anyways, the dead time is dictated by the turn OFF of Q1B because it has the longest delay.

Dead Time Calculation

The dead time is dictated by the upper MOSFET because it has the longest delay.

$\text{CISS\_Q2} := 73\text{pF}$

CISS of Q2. This must be maximum but the datasheet only gives the typical value.

$\text{RgQ2} := 2.2\Omega$

Max gate resistance of Q2. The specified value in the datasheet is 2.2 ohm typical.

$\text{VGS\_Q2threshold\_min} := 0.8\text{V}$

Minimum VGS threshold of Q2

$\text{VphaseA} := 3.3\text{V}$

$$\text{tdecay\_Q2gate} := -\text{CISS\_Q2}\cdot\text{RgQ2}\cdot\ln\left(\frac{\text{VGS\_Q2threshold\_min}}{\text{VphaseA}}\right)$$

$\text{tdecay\_Q2gate} = 0.228\,\text{ns}$

$\text{COSS\_Q2} := 25\text{pF}$

COSS of Q2. The datasheet only gives 7pF as the typical values. 25pF is taken from another vendor which is the maximum value.

$\text{R1} := 330\Omega$

Value of pull-up resistor

$\text{V12VMotor} := 12\text{V}$

12V Motor supply level

$\text{VSG\_Q1B\_min} := 1.2\text{V}$

Minimum source to gate threshold of Q1B

$$\text{trise\_Q2drain} := -\text{COSS\_Q2}\cdot\text{R1}\cdot\ln\left(1 - \frac{\text{V12VMotor} - \text{VSG\_Q1B\_min}}{\text{V12VMotor}}\right)$$

$\text{trise\_Q2drain} = 18.996\,\text{ns}$

$\text{CISS\_Q1B} := 970\text{pF}$

CISS of Q1B

$\text{RgQ1B} := 11\Omega$

Maximum gate resistance of Q1B

$$\text{tdecay\_Q1Bgate} := -\text{CISS\_Q1B}\cdot\text{RgQ1B}\cdot\ln\left(\frac{\text{VSG\_Q1B\_min}}{\text{V12VMotor}}\right)$$

$\text{tdecay\_Q1Bgate} = 24.569\,\text{ns}$

$\text{COSS\_Q1B} := 120\text{pF}$

COSS of Q1B. This must be maximum but the datasheet give only the typical value

$\text{RLoad} := 12\Omega$

Equivalent load considering 1A. 1A load has longer COSS charge than 2A load

Based on the requirements on the word document, the normal current is can be up to 1A. What is the minimum current? The minimum current will correspond to a higher resistance and the worst charge time for the COSS of Q1B.

$$\text{trise\_Q1Bdrain} := 4.990832666800076037\cdot\text{COSS\_Q1B}\cdot\text{RLoad}$$

$\text{trise\_Q1Bdrain} = 7.187\,\text{ns}$

$\text{MCUdelay} := 300\text{ns}$

This is the assumed microntroller execution delay. You can modify the comptation using exact delay in the excel dead time calculator I provided.

$$\text{toff\_Q1B\_total} := \text{tdecay\_Q2gate} + \text{trise\_Q2drain} + \text{tdecay\_Q1Bgate} + \text{trise\_Q1Bdrain} + \text{trise\_Q1Bdynamic} + \text{MCUdelay}$$

$\text{toff\_Q1B\_total} = 374.979\,\text{ns}$

This is the overall delays not considering the stray capacitances. Stray capacitances will make the delay much longer. Failure to consider this one make the FETs conduction to overlap. The trace resistance must be considered as well.

Total Delay with Parasitics

NOTE : STRAY CAPACITANCE IS VERY DIFFICULT TO MEASURE. I AM USING BELOW VALUES BASED ON THE USUAL VALUE USED IN ANALYSIS.

$\mathrm{CISS\_Q2\_stray} := 300\mathrm{pF}$ Assumed stray capacitance. You can change this value in the tool I provided.

$\mathrm{RgQ2\_trace} := 1\Omega$ Assumed trace resistance

$$\mathrm{tdecay\_Q2gate\_withStray} := -(\mathrm{CISS\_Q2} + \mathrm{CISS\_Q2\_stray})\cdot(\mathrm{RgQ2} + \mathrm{RgQ2\_trace})\cdot\ln\left(\frac{\mathrm{VGS\_Q2threshold\_min}}{\mathrm{VphaseA}}\right)$$

$\mathrm{tdecay\_Q2gate\_withStray} = 1.691\,\mathrm{ns}$

$\mathrm{COSS\_Q2\_stray} := 300\mathrm{pF}$ Assumed stray capacitance. You can change this value in the tool I provided.

$$\mathrm{trise\_Q2drain\_withStray} := -(\mathrm{COSS\_Q2} + \mathrm{COSS\_Q2\_stray})\cdot \mathrm{R1}\cdot\ln\left(1 - \frac{\mathrm{V12VMotor} - \mathrm{VSG\_Q1B\_min}}{\mathrm{V12VMotor}}\right)$$

$\mathrm{trise\_Q2drain\_withStray} = 246.952\,\mathrm{ns}$

$\mathrm{CISS\_Q1B\_stray} := 300\mathrm{pF}$ Assumed stray capacitance. You can change this value in the tool I provided.

$\mathrm{RgQ1B\_trace} := 1\Omega$

$$\mathrm{tdecay\_Q1Bgate\_withStray} := -(\mathrm{CISS\_Q1B} + \mathrm{CISS\_Q1B\_stray})\cdot(\mathrm{RgQ1B} + \mathrm{RgQ1B\_trace})\cdot\ln\left(\frac{\mathrm{VSG\_Q1B\_min}}{\mathrm{V12VMotor}}\right)$$

$\mathrm{tdecay\_Q1Bgate\_withStray} = 35.091\,\mathrm{ns}$

$\mathrm{COSS\_Q1B\_stray} := 300\mathrm{pF}$ Assumed stray capacitance. You can change this value in the tool I provided.

$$\mathrm{trise\_Q1Bdrain\_withStray} := 4.990832666800076037\cdot(\mathrm{COSS\_Q1B} + \mathrm{COSS\_Q1B\_stray})\cdot \mathrm{RLoad}$$

$\mathrm{trise\_Q1Bdrain\_withStray} = 25.154\,\mathrm{ns}$

$$\text{toff\_Q1B\_total\_withStray} := \text{tdecay\_Q2gate\_withStray} + \text{trise\_Q2drain\_withStray} + \text{tdecay\_Q1Bgate\_withStray} \ldots + \text{trise\_Q1Bdrain\_withStray} + \text{MCUdelay} + \text{trise\_Q1Bdynamic}$$

$\text{toff\_Q1B\_total\_withStray} = 632.889\ \text{ns}$

This is the overall delays considering the stray capacitances. The minimum dead time must be higher than this value.

Let us consider a 50% margin for instance, the dead time would be

$\text{Margin} := 60\%$

Declared margin

$\text{DeadTime} := \text{toff\_Q1B\_total\_withStray}\cdot(1 + \text{Margin})$

$\text{DeadTime} = 1.013 \times 10^{3}\ \text{ns}$

This is the computed dead time plus margin

NOTE :
You can do recomputations in the excel calculator I made in case you change parts.