Improving Buck Converter EMI Performance

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Introduction

Objective:

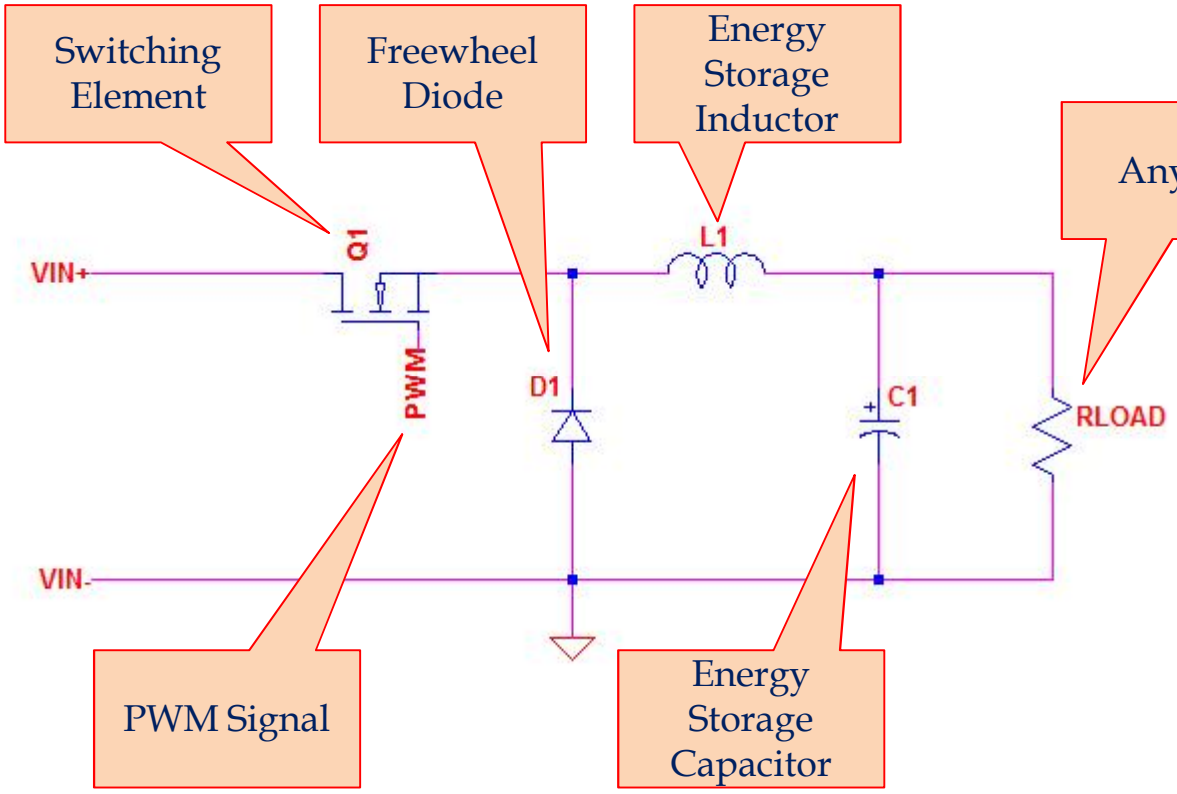
- To improve buck converter EMI performance by starting from a good design planning, identifications of critical current loop and have it minimized, identifying and minimizing critical nodes (spikes and ringing) and applying ready fixes in the layout.

Introduction

Topics:

- Typical Buck Converter Circuit
- Typical Buck Converter Operation
- Buck Converter Current Loops
- Buck Converter Critical Current Loop
- Effects of Critical Current Loop
- Minimizing Critical Current Loop Area
- Identifying Noisy Nodes
- Minimizing Buck Converter Noisy Node
- Minimizing Ground Loops
- Using Wide Return Paths and Ground Plane
- Isolate Silent Nodes from the Noisy Ones
- Reviewing What We have Learned

Typical Buck Converter Circuit



Operation Modes

✓ Continuous Conduction Mode (CCM)

Click here

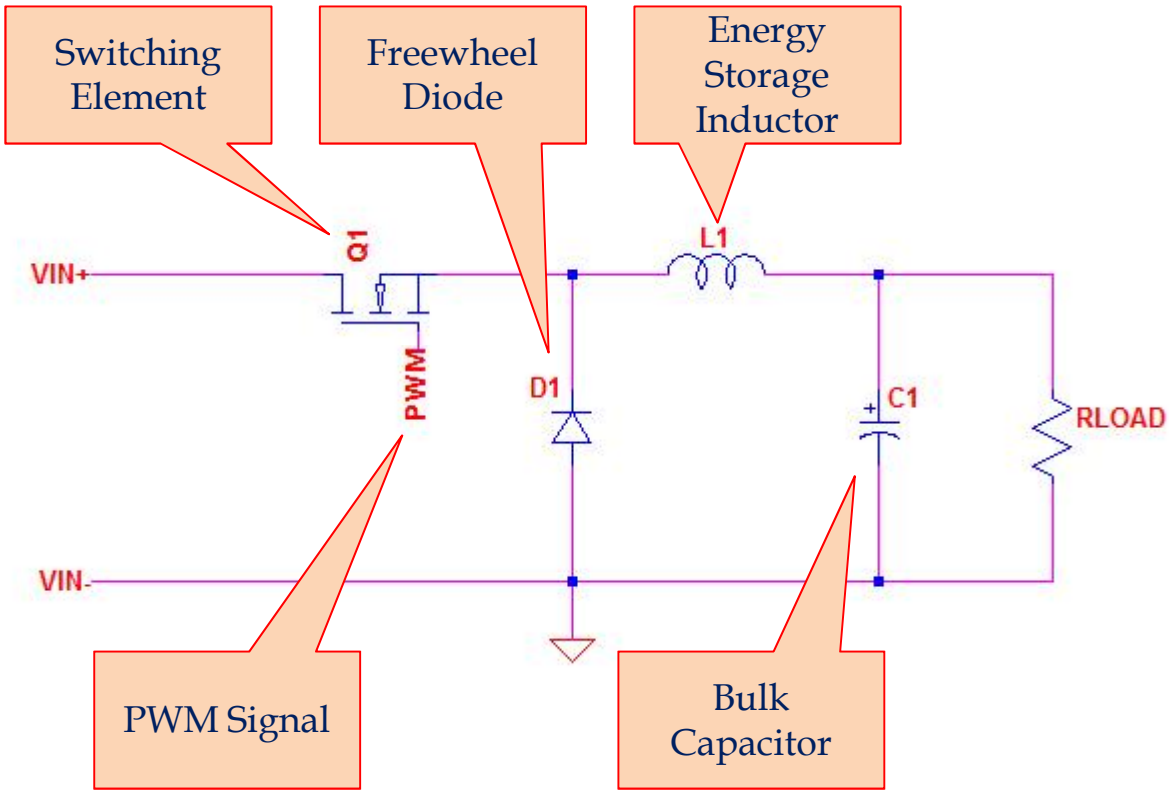
✓ Discontinuous Conduction Mode (DCM)

Click here

✓ Transition Mode or Boundary Mode (TM)

Click here

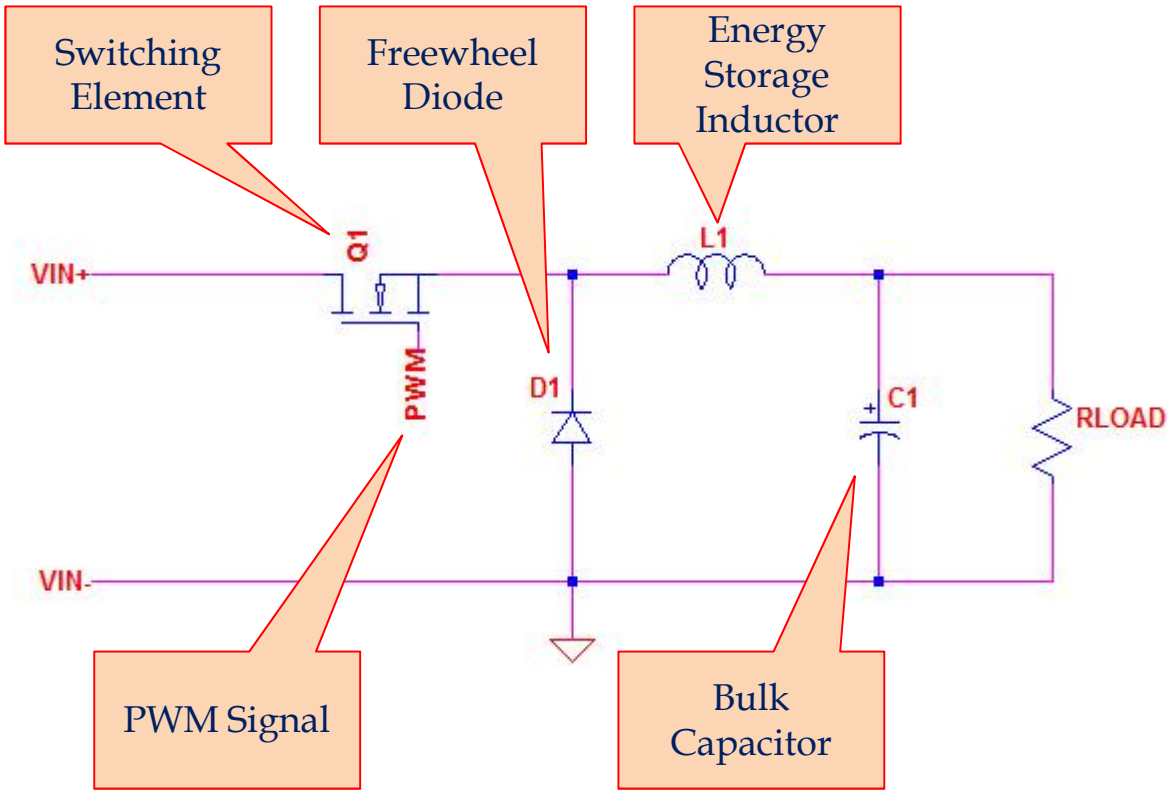
Typical Buck Converter Operation



✓When Q1 is ON, D1 is OFF and the inductor L1 will charge as well as the capacitor C1. The load gets its power from the input.

✓When Q1 is OFF, L1 will discharge and diode D1 will conduct. Both the energy stored in L1 and C1 will supply the load during this time.

Typical Buck Converter Operation



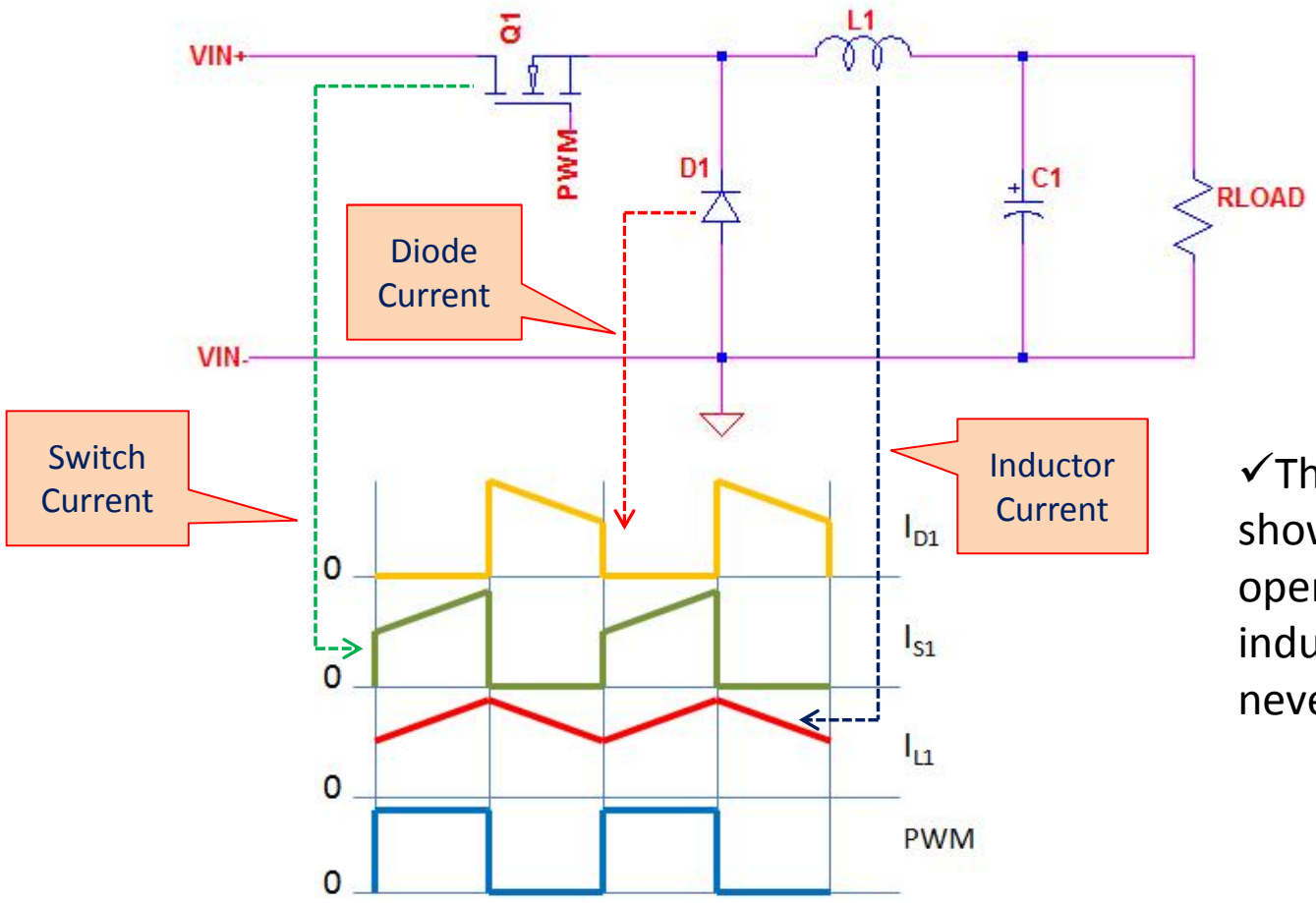
✓The maximum output level is just the same to the input (ideally)

✓The output will keep regulated by controlling the duty cycle of the PWM on Q1

✓The current in the inductor is can be continuous, discontinuous and just in the boundary

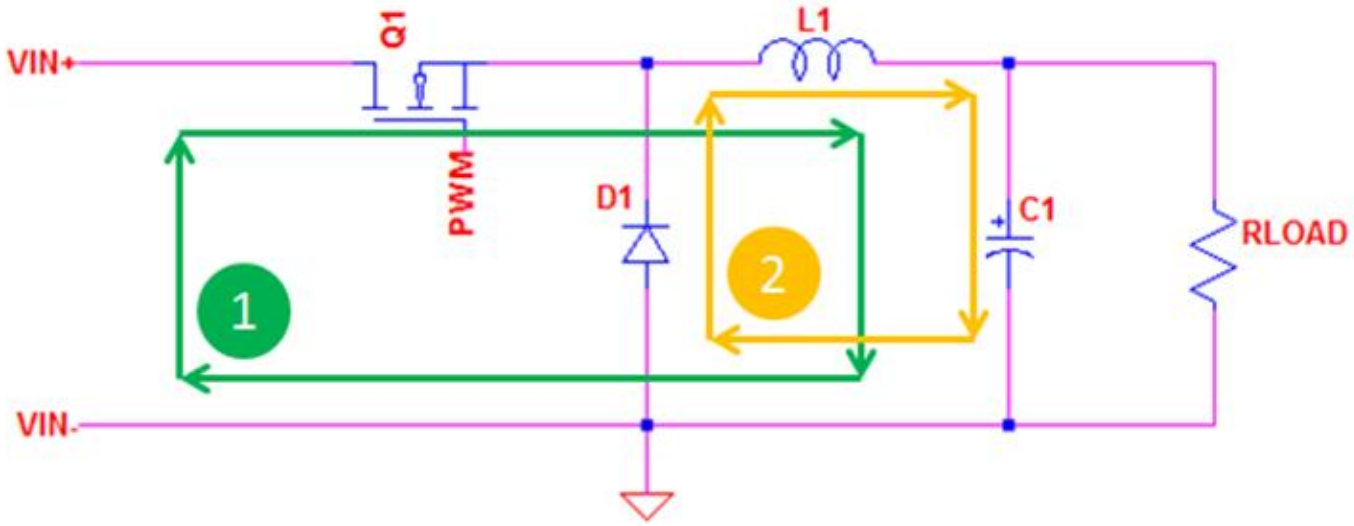
✓Click here to know how duty cycle is derived

Typical Buck Converter Operation



✓The waveform shows a CCM operation since the inductor current never touches zero

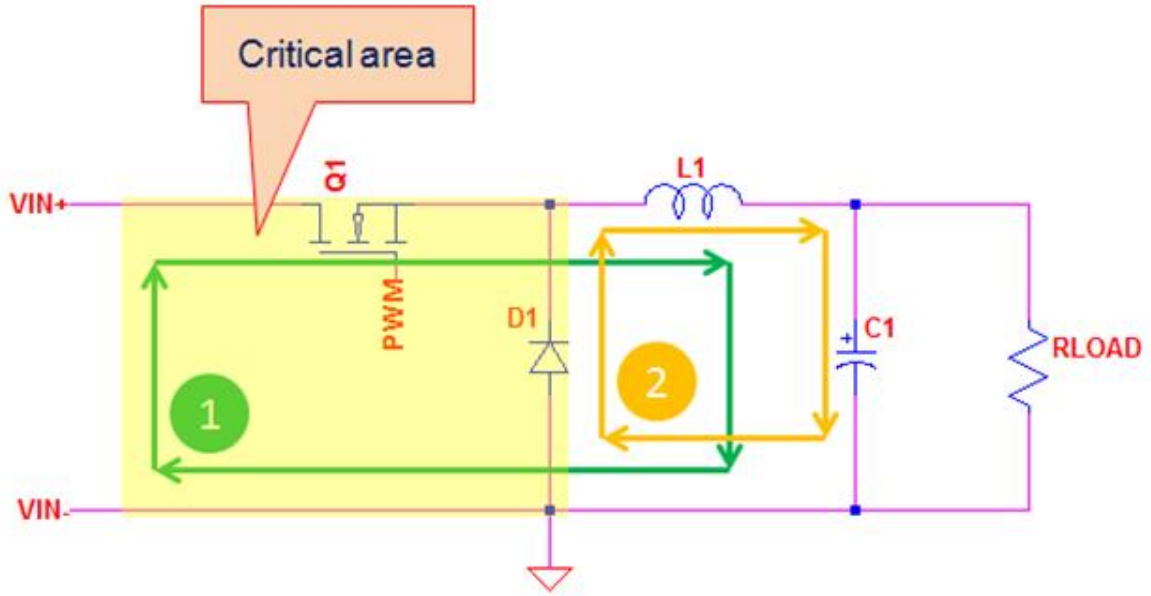
Buck Converter Current Loops



✓The first current loop is happening when Q1 is ON while diode is OFF

✓The second current loop is formed when Q1 is OFF and diode is ON

Buck Converter Critical Current Loop

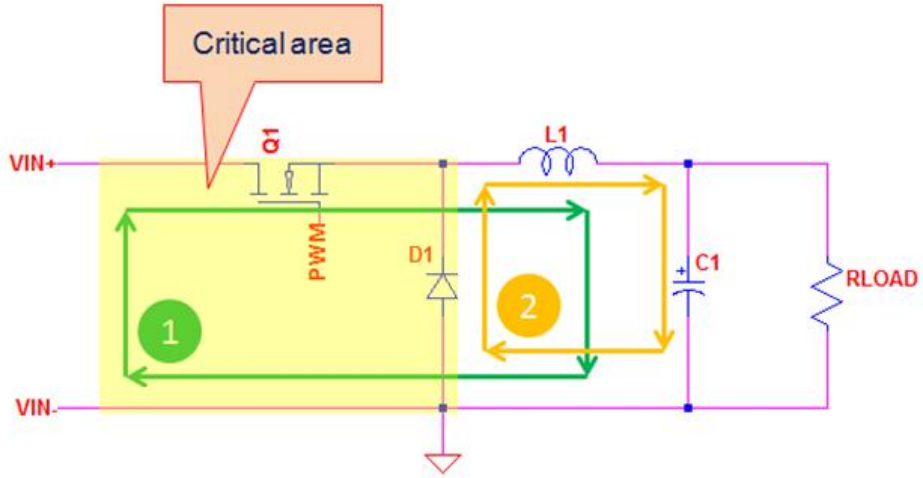


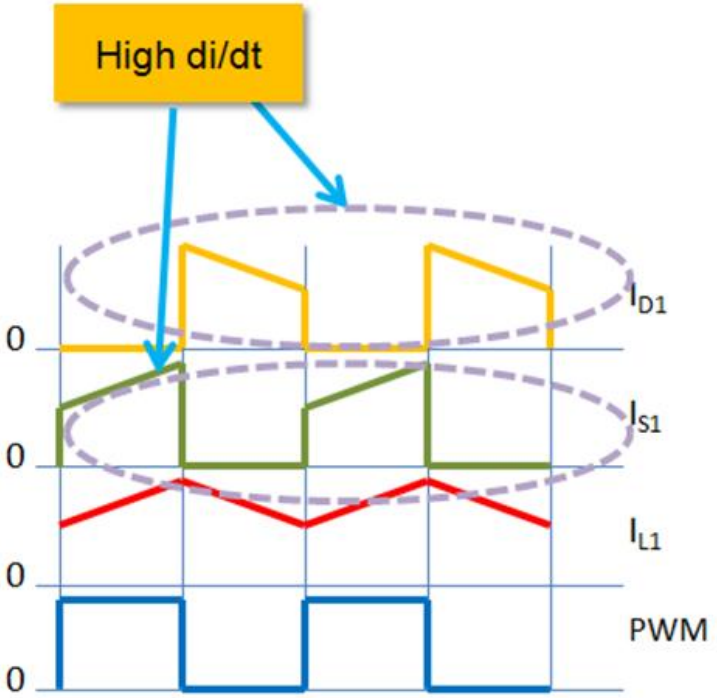
✓The critical current loop is the one that has the highest change in current di/dt

✓For a buck converter, the shaded region has the highest di/dt

✓Most of the times, the area that has inductor is not the critical since buck converter usually operated at CCM wherein the current on the inductor never reaches zero

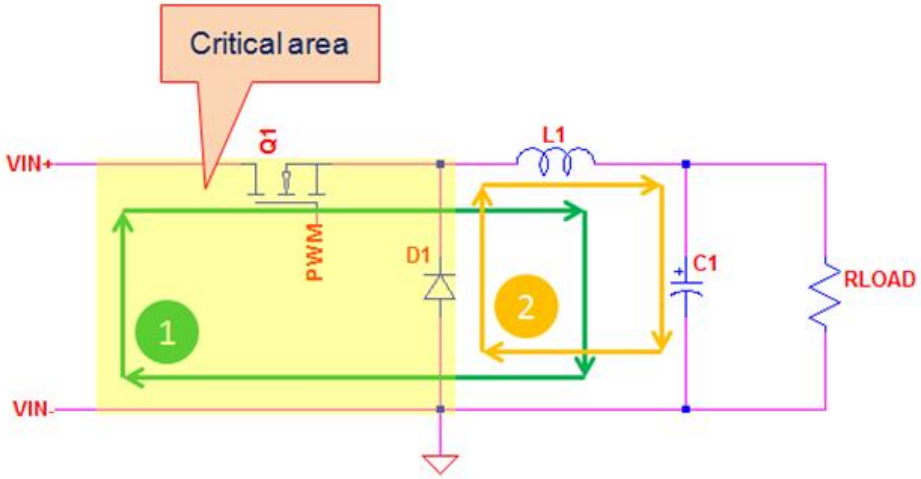
Buck Converter Critical Current Loop



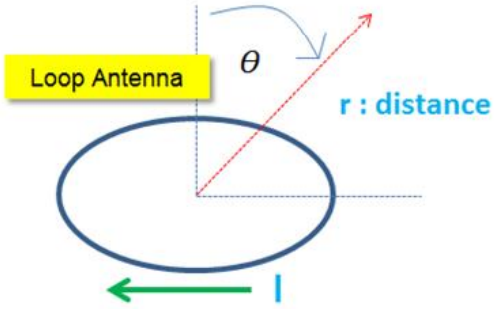


✓The waveform above shows a CCM operation wherein the current on the inductor never reaches zero.
✓The current in the MOSFET and the diode has the highest di/dt making the area bounded by the two a critical area.

Effects of Critical Current Loop



✓Critical current loop will form a strong unintentional loop antenna when not treated. This loop antenna has a field strength that is directly proportional to the area.

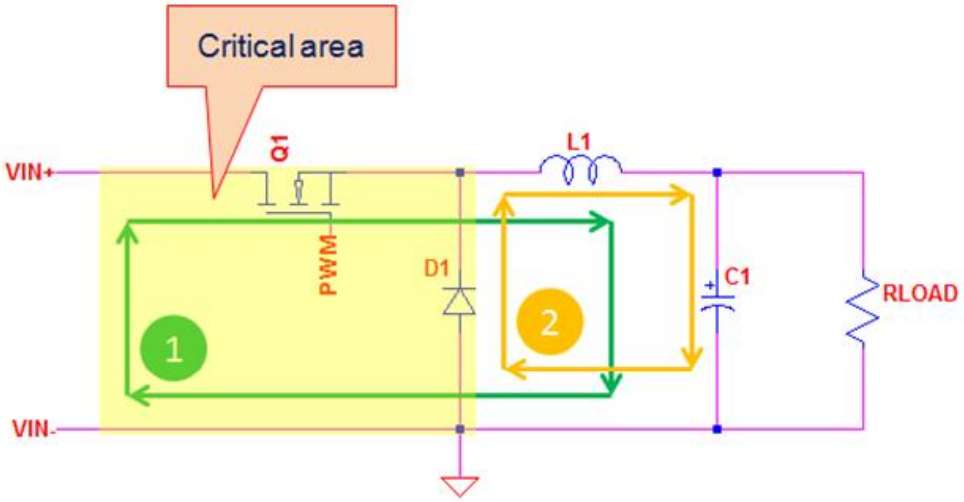


$$E = \frac{131.6 \times 10^{-16}(f^2 \times A \times I)sin\theta}{r}$$

A: Area of the loop
f: switching frequency
I: Current
r: distance
L: length

✓The higher the E field the higher the radiation will be. Radiated EMI will be compromised.

Effects of Critical Current Loop

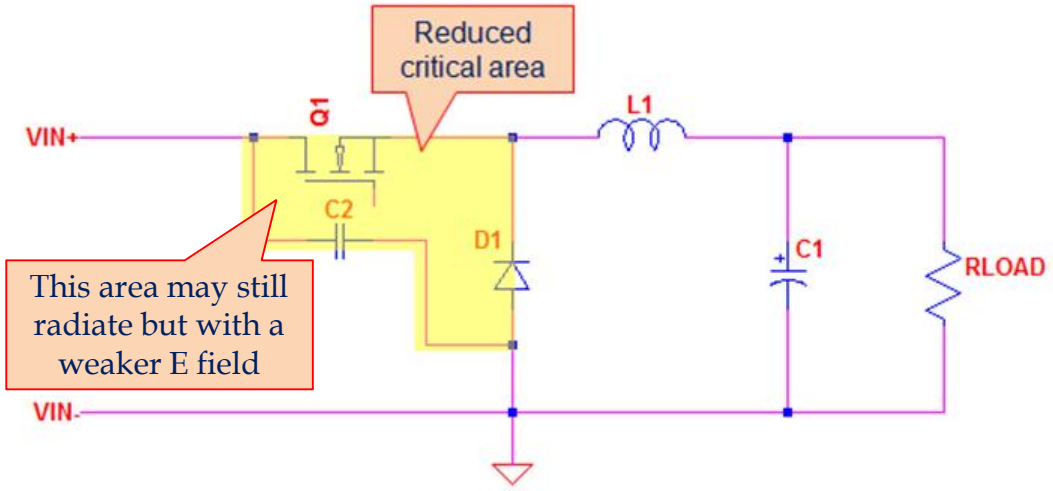


✓Critical current loop has the highest di/dt. A large loop will have a high stray inductance. The presence of a high inductance together with a high di/dt will give a large noise voltage

$$V_{NOISE} = L_{stray} \times di/dt$$

✓The presence of this noise voltage will introduce an issue on conducted EMI as well since the differential mode currents will travel to the source of the converter especially if this is an AC-DC buck converter.

Minimizing Critical Current Loop Area



✓A bypass capacitor will provide a short return path for the noise

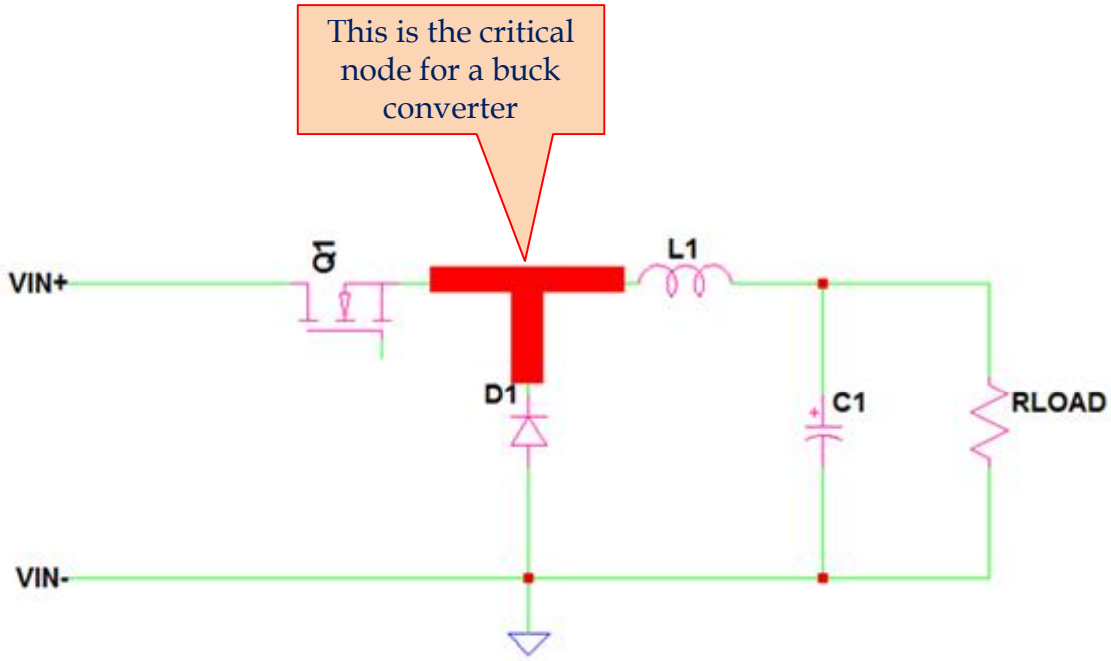
✓At high frequencies, the impedance of a capacitor will be very low. Noise is mostly high frequency since it is due to the current harmonics of the switching element that present in few to some frequency multiples of the nominal switching frequency

✓An effective way of minimizing the critical area is by using a bypass capacitor

✓The figure shows how the bypass capacitor to be placed in a noisy section of a buck converter

✓PCB layout must be properly done to make this solution effective; such as eliminating capacitor leads thus MLCCs are preferred, using a wide and return path and selecting a lower ESR bypass cap

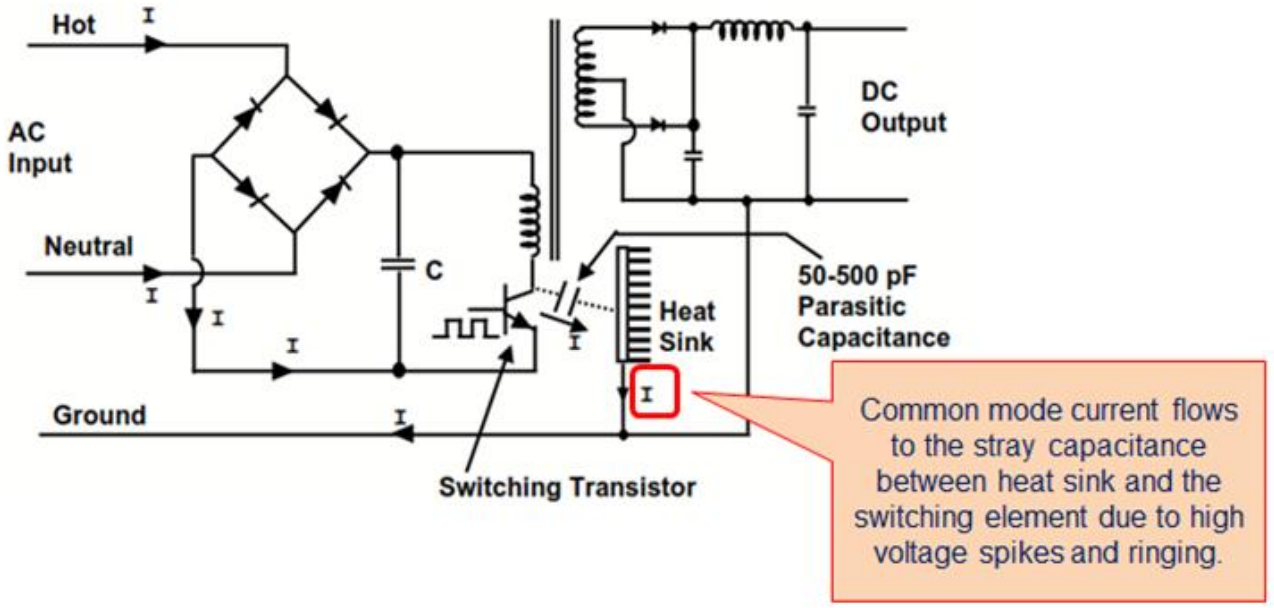
Identifying Noisy Nodes



✓This is a noisy node. It is important to minimize stray capacitance in this area. A larger stray capacitance will create a bigger noise current as defined by the equation below

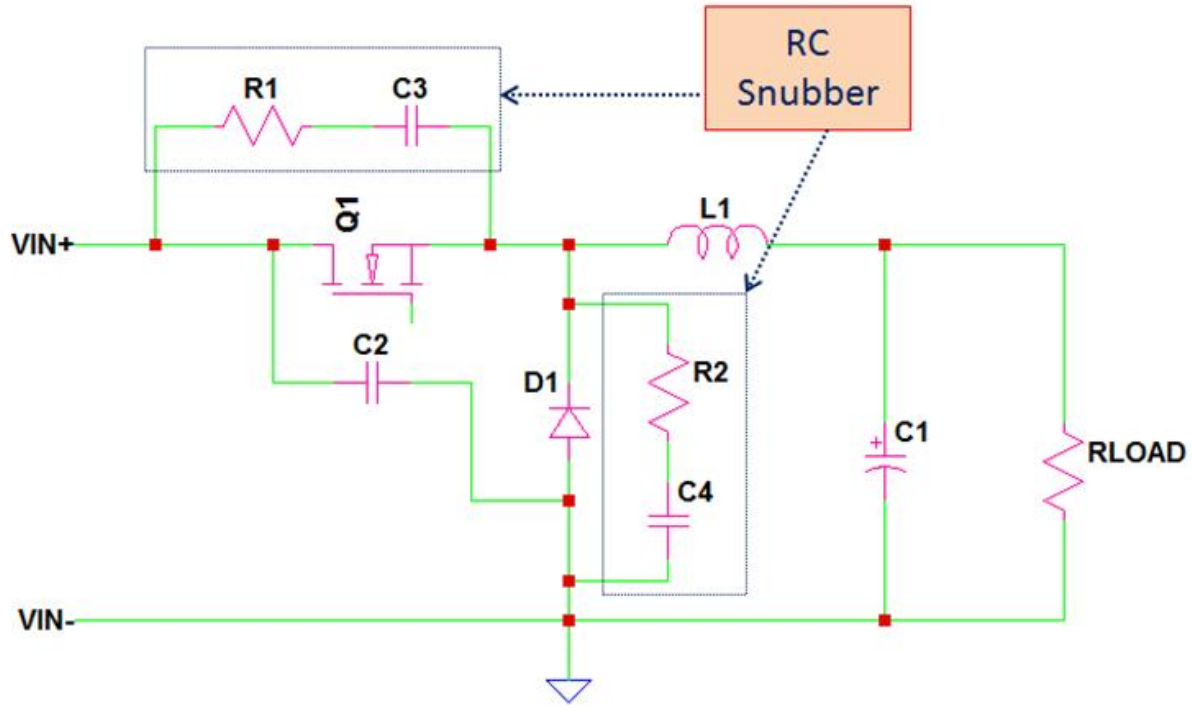
$$I_{NOISE} = C_{STRAY} \times dv/dt$$

Identifying Noisy Nodes



✓Excessive voltage spikes create a common mode current through the stray capacitance between the MOSFET and the heat sink

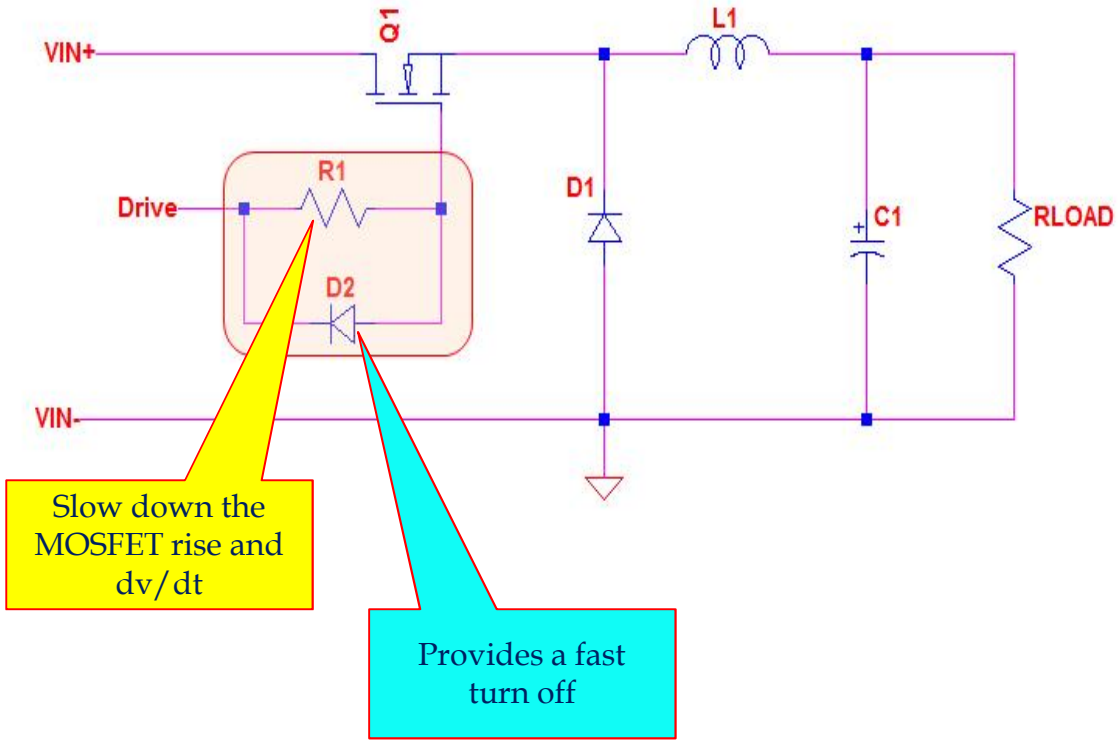
Minimizing Buck Converter Noisy Node



✓Adding a snubber is a good way of clipping the voltage spikes and ringing on both the MOSFET and the diode

✓However, there will be additional loss due to the dissipation of the resistor. Check the efficiency and make a tradeoff between spike suppression level and loss

Minimizing Buck Converter Noisy Node

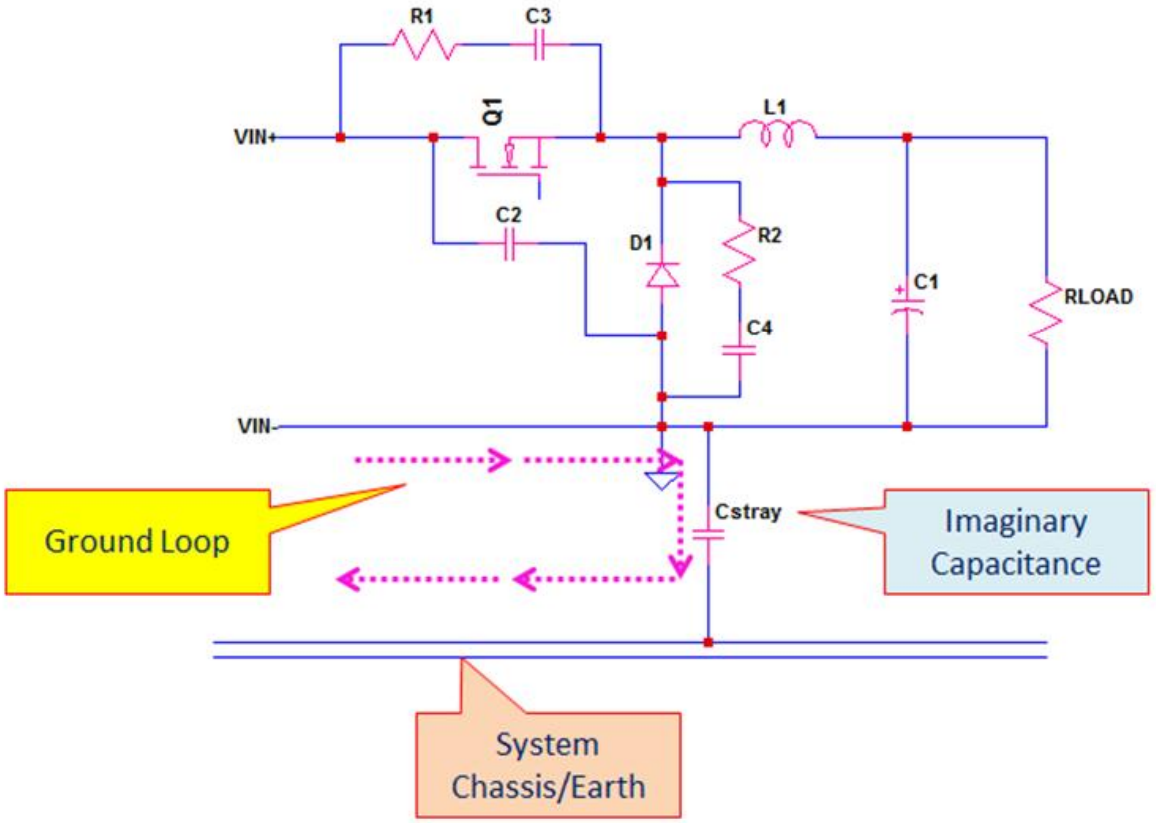


✓Slowing the MOSFET rise may also help minimize the spike and ringing in the drain.

✓It will lower the MOSFET dv/dt

✓Again, efficiency may be compromised for too large gate resistance

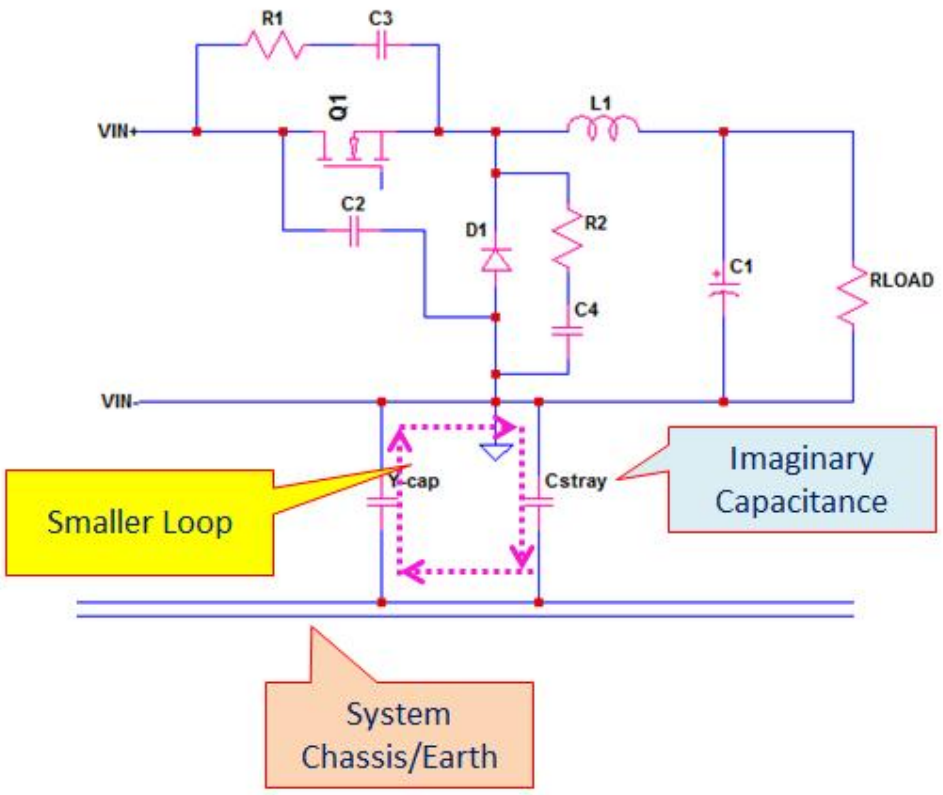
Minimizing Ground Loops



✓Current flows to the system ground from the local ground due to a stray capacitance linking both grounds

✓Actually, the stray capacitance will remain an open circuit as long as there is no change in voltage that makes its impedance low and allow current to flow (I = C dv/dt)

Minimizing Ground Loops



✓Using a **Y-cap** makes the wide ground loop a narrow one

✓With the addition of the Y-cap, the noise current will have its short return path. The current loop becomes smaller and also its radiating effect will become weaker. The noise current will no longer go back to the power line (maybe there is still but with a lesser effect) and conducted EMI will greatly improve.

Using Wide Return Paths and Ground Plane

✓Large return path or a ground plane is very important to help improve buck converter EMI performance

✓A larger return path also minimizes stray inductances that will create noise voltage

$$(V_{NOISE} = L_{STRAY} \times di/dt)$$

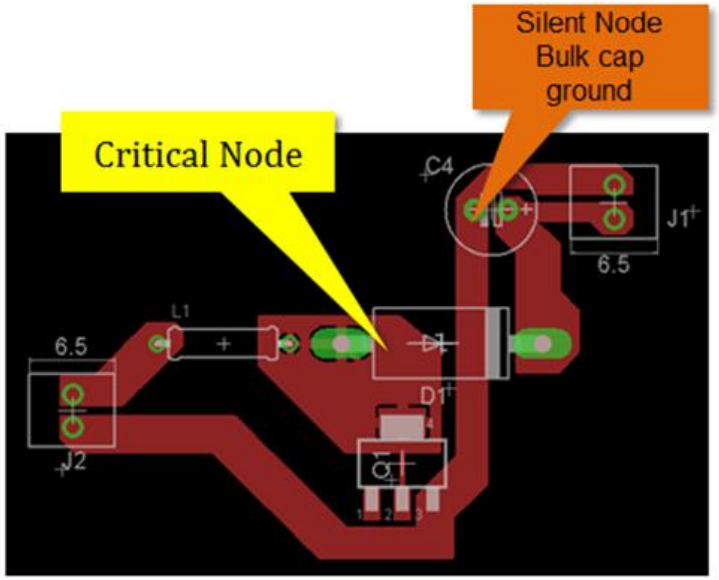
✓Noise is just like signal; it likes to flow in a less opposing path.

✓Some tests results concluded that when a ground plane below the high di/dt path is cut the EMI increases

Isolate Silent Nodes from the Noisy Ones

✓The silent node is the one where the bulk capacitor is connected. A capacitor will simply not allow a change in voltage. All signals or other circuits are getting their reference ground on the capacitor. Keep these silent nodes from the critical node identified in the previous slide

✓Keep also the sensitive circuits away from the noisy nodes, such MCUs, DSPs, FPGAs and others. Also keep these circuits or devices from the power parts; MOSFET, diode and the inductor for these may introduce noise to them.



✓This is a bad layout. The silent node passes near the noisy node.

Reviewing What We Have Learned

✓Critical current loop area must be minimized if not totally been eliminated to weaken the strength of radiation
✓Critical current loop area acts as a loop antenna which E field strength is directly proportional to the magnitude of current, frequency and the area
✓A high di/dt when pass an inductive path will generate a noise voltage with a magnitude

$$V_{NOISE} = L_{STRAY} \times di/dt$$

✓A very simple way to minimize critical current loop area is by using a bypass capacitor
✓Critical voltage node has high dv/dt and must be minimized to minimize common mode currents that flows through the heat sink with a magnitude

$$I_{NOISE} = C_{STRAY} \times dv/dt$$

Reviewing What We Have Learned

Reference:

http://electronicsbeliever.com/buck-converter-emi-performance/

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